



PTO/SB/21 (09-04)

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FORM**

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Total Number of Pages in This Submission

Application Number

10/810,963

Filing Date

03/26/2004

First Named Inventor

Thomas Rueckes et al.

Art Unit

2818

Examiner Name

TBA

Attorney Docket Number

112020.146US2 NAN-22

**ENCLOSURES (Check all that apply)**

<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to TC
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<input type="checkbox"/> Reply to Missing Parts/ Incomplete Application	<input type="checkbox"/> Remarks	
<input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	1. PTO Form (4 pgs.)	
	2. 30 Publications	

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Firm Name	Wilmer Cutler Pickering Hale and Dorr LLP		
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Printed name	Peter M. Dichiaro		
Date	01/03/2005	Reg. No.	38,005

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PATENT

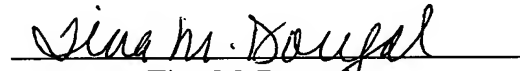
**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: Rueckes, et al.  
Application No.: 10/810,963 Examiner: Unknown  
Filed: March 26, 2004 Group Art Unit: 2818  
For: Non-Volatile RAM Cell and Array Using Nanotube Switch Position  
for Information State  
Atty. Docket No.: 112020.146 US2 (NAN-22)

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Sir:

Applicants and their legal representatives hereby make of record on the attached Form PTO-1449 the following publications which are known to them and considered warranting disclosure under 37 C.F.R. §1.56 and 1.97-98.

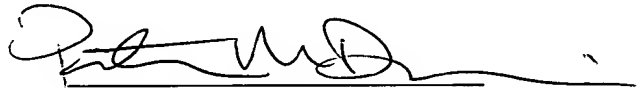
Copies of the publications listed on the attached Form PTO-1449, with the exception of cited U.S. Patents and U.S. published applications, are submitted herewith. It is respectfully requested that the Examiner initial and return a copy of the subject Form PTO-1449 with the next Patent Office communication.

The submission of these publications does not constitute a representation by the Applicants that a search has been made or that no better art exists and does not constitute an admission that the listed publications are material or constitute "prior art." Applicants reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed publications, should one or more of the publications be applied against the claims of the present application.

It is Applicants' belief that the Information Disclosure Statement is being filed prior to the mailing date of the first Office Action on the merits and, therefore, no fee is due. However, in the event a fee is due, please charge any fee deficiency or credit any overpayment to Deposit Account No. 08-0219.

Respectfully submitted,

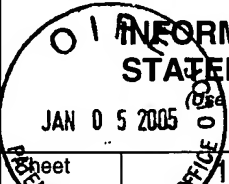
Dated: January 3, 2005

A handwritten signature in dark ink, appearing to read "Peter M. Diciara", written over a horizontal line.

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Substitute for form 1449/PTO		<b>Complete if Known</b>	
		Application Number	10/810,963
		Filing Date	March 26, 2004
		First Named Inventor	Rueckes, Thomas et al.
		Art Unit	2818
		Examiner Name	TBA
		Attorney Docket Number	112020.146US2 NAN-22
Sheet 1	of 4		

## U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
		US-2004/0085805A1	05-06-2004	SEGAL et al.	
		US-2004/0159833A1	08-19-2003	RUECKES et al.	
		US-2004/0164289A1	08-26-2003	RUECKES et al.	
		US-2004/0191978A1	09-30-2004	RUECKES et al.	
		US-2004/0214366 A1	10-28-2004	SEGAL et al.	
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		US-2003/0234407A1	12-25-2003	VOGELI et al.	
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		US-6,128,214	10-03-2000	KUEKES et al.	
		US-6,159,620	12-12-2000	HEATH et al.	
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		US-6,232,706	05-15-2001	DAI et al.	
		US-6,445,006	09-03-2002	BRANDES et al.	

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Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>				Application Number	10/810,963
				Filing Date	March 26, 2004
				First Named Inventor	Rueckes, Thomas et al.
				Art Unit	2818
				Examiner Name	TBA
Sheet	2	of	4	Attorney Docket Number	112020.146US2 NAN-22

	US-6,518,156 B1	02-11-2003	CHEN	
	US-6,559,468 B1	05-06-2003	KUEKES et al.	
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	US-6,706,402	03-16-2004	RUECKES et al.	
	US-6,750,471B2	06-15-2004	BETHUNE et al.	
	US-6,759,693	07-06-2004	VOGELI et al.	
	US-6,673,424 B1	01-06-2004	LINDSAY	
	US-6,774,052	08-10-2004	VOGELI et al.	
	US-6,781, 166 B1	08-24-2004	LIEBER et al.	
	US-6,784,028	08-31-2004	RUECKES et al.	

## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		WO 01/44796 A1	06-21-2001	Board of Trustees of the Leland Stanford Junior. University.	
		WO 01/03208 A1	01-11-2001	President and Fellows of Harvard College	

## NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	A1	CHOI, W. B. et al., "Carbon-nanotube-based nonvolatile memory with oxide-nitride-film and nanoscale channel." <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(2) 275-277.	
	A2	DEQUESNES, M. et al., "Calculation of pull-in voltages for carbon-nanotube-based nanoelectromechanical switches." <i>Nanotechnology</i> , 2002, Vol. 13, 120-131.	
	A3	DEQUESNES, M. et al., "Simulation of carbon nanotube-based nanoelectromechanical switches." <i>Computational Nanoscience and Nanotechnology</i> , 2002, 383-386.	

Examiner Signature	Date Considered
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				Examiner Name	TBA
Sheet	3	of	4	Attorney Docket Number	112020.146US2 NAN-22

A4	WOLF, S., Silicon Processing for the VLSI Era; Volume 2 – Process Integration, Multi-Level-Interconnect Technology for VLSI and ULSI, 1990, Section 4.3 Materials for Multilevel Interconnect Technologies, pp. 189-191, Lattice Press, Sunset Beach	
A5	WOLF, S., Silicon Processing for the VLSI Era; Volume 2 – Process Integration, 1990, Section 4.7 Manufacturing Yield and Reliability Issues of VLSI Interconnects, pp. 260-273, Lattice Press, Sunset Beach	
A6	ROBINSON, L.A.W., "Self-Aligned Electrodes for Suspended Carbon Nanotube Structures." <i>Microelectronic Engineering</i> , 2003, Vols. 67-68, 615-622.	
A7	TOUR, J. M. et al., "NanoCell Electronic Memories." <i>J. Am. Chem Soc.</i> , 2003, Vol. 125, 13279-13283.	
A8	RUECKES, T., et al., "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing" <i>Science</i> , 2000, Vol. 289, 94-97.	
A9	FAN, S. et al., "Carbon nanotube arrays on silicon substrates and their possible application." <i>Physica E</i> , 2000, Vol. 8, 179-183.	
A10	ZHAN, W. et al., "Microelectrochemical Logic Circuits." <i>J. Am. Chem. Soc.</i> , 2003, Vol. 125, 9934-9935.	
A11	SOH, H. T. et al., "Integrated nanotube circuits: Controlled growth and ohmic contacting of single-walled carbon nanotubes." <i>Appl. Phys. Lett.</i> , 1999, Vol. 75(5) 627-629.	
A12	KINARET, J.M. et al., "A carbon-nanotube-based nanorelay", <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(8) 1287-1289.	
A13	FRANKLIN, N. R. et al., "Integration of suspended carbon nanotube arrays into electronic devices and electromechanical systems." <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(5) 913-915.	
A14	AVOURIS, P., "Carbon nanotube electronics," <i>Chem. Physics</i> , 2002, Vol. 281, pp. 429-445.	
A15	DAI, H. et al., "Controlled Chemical Routes to Nanotube Architectures, Physics, and Devices." <i>J. Phys. Chem. B</i> , 1999, Vol. 103, 111246-11255.	
A16	HOMMA, Y. et al., "Growth of Suspended Carbon Nanotubes Networks on 100-nm-scale Silicon Pillars." <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(12) 2261-2263.	
A17	AJAYAN, P.M., et al., "Nanometre-size tubes of carbon." <i>Rep. Prog. Phys.</i> , 1997, Vol. 60, 1025-1062.	
A18	SREEKUMAR, T.V., et al., "Single-wall Carbon Nanotube Films", <i>Chem. Mater.</i> 2003, Vol. 15, 175-178.	

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Sheet	4	of	4	Attorney Docket Number	112020.146US2 NAN-22

	A19	VERISSIMO-ALVES, M. et al., "Electromechanical effects in carbon nanotubes: <i>Ab initio</i> and analytical tight-binding calculations." <i>Phys. Rev. B</i> , 2003, Vol. 67, 161401-1 - 161401-4.	
	A20	FUHRER, M.S. et al., "High-Mobility Nanotube Transistor Memory." <i>Nano Letters</i> , 2002, Vol. 2(7) 755-759.	
	A21	RADOSAVLJEVIC, M. et al., "Nonvolatile molecular memory elements based on ambipolar nanotube field effect transistors." <i>Nano Letters</i> , 2002, Vol. 2(7) 761-764.	
	A22	FARAJIAN, A. A. et al., "Electronic transport through bent carbon nanotubes: Nanoelectromechanical sensors and switches." <i>Phys. Rev. B</i> , 200, Vol. 67, 205423-1 - 205423-6.	
	A23	FISCHER, J.E. et al., "Magnetically aligned single wall carbon nanotube films: Preferred orientation and anisotropic transport properties." <i>Journal of Appl. Phys.</i> , 2003, Vol. 93(4) 2157-2163.	
	A24	LEE, K.H. et al., "Control of growth orientation for carbon nanotubes." <i>Appl. Phys. Lett.</i> , 2003, 82 (3) 448-450.	
	A25	CASAVANT, M.J. et al., "Neat macroscopic membranes of aligned carbon nanotubes." <i>Journal of Appl. Phys.</i> , 2003, Vol. 93(4) 2153-2156.	
	A26	AMI, S. et al., "Logic gates and memory cells based on single C <sub>60</sub> electromechanical transistors." <i>Nanotechnology</i> , 2001, Vol. 12, 44-52.	
	A27	DEHON, A., "Array-Based Architecture for FET-Based, Nanoscale Electronics." <i>IEEE Transactions on Nanotechnology</i> , 2003, Vol. 2(1) 23-32.	
	A28	TANS, S. et al., "Room-temperature transistor based on a single carbon nanotube." <i>Nature</i> , 1998, Vol. 393, 49-52.	
	A29	CUI, J.B. et al., "Carbon Nanotube Memory Devices of High Charge Storage Stability." <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(17) 3260-3262.	

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